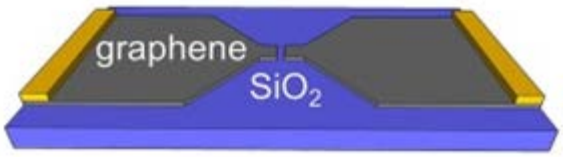
Master Thesis

Nanometer scale SiO_x resistive switches for neuromorphic applications

The laboratory "Transport at Nanoscale Interfaces" at Empa Dübendorf is looking for strong candidates with a background in nanoscience, physics, or electrical engineering for a master thesis research project.

While current CMOS technology is reaching the sub-10 nm regime, a broad consensus arises that a further boosting in computational power will primarily rely on novel circuit elements exhibiting an in-creased functional complexity, as well as on massively parallel, beyond-von Neumann architectures benefiting from an improved interconnectivity of their building blocks [1]. Networks of two-terminal resistance change random access memory devices (Re-RAMs) are outstanding candidates as such elements are expected to be scalable below 10 nm due to the filamentary nature of their resistive switching and, at the same time, they also offer multi-bit operations via the analogue tuneability of their resistance states.



In the current research project we investigate the switching dynamics of truly nanometer sized, SiO_x based ReRAM devices mounted with graphene electrodes. We have shown recent-ly [2] that, unlike most phase change type memories, such units can be programed by unipo-lar voltage pulses, they are capable of non-volatile data storage at zero bias and the stored information is accessible at low voltage levels. In order to uncover the physical mechanism responsible for the above, complex switching characteristics, a series of structural and transport characterizations are planned. These will provide the master student with the op-portunity to gain hands-on experience in a broad range of modern nanofabrication & meas-urement techniques including micro- and nanofabrication in a cleanroom environment, elec-tron-beam and scanning probe microscopy as well as low-noise transport experiments.

For applications (with motivation and CV) and more information please contact Dr. Miklos Csontos (miklos.csontos@empa.ch).

References

[1] M. Di Ventra and Y. V. Pershin. The parallel approach. Nature Physics **9**, 200-2002 (2013).

[2] L. Posa *et al*. Multiple Physical Time Scales and Dead Time Rule in Few-Nanometers Sized Graphene−SiOx-Graphene Memristors. Nano Letters **17**, 6783-6789 (2017).